

**REMARKS**

At the time of the Office Action dated June 17, 2004, claims 1-6 were pending. Applicant acknowledges, with appreciation, the Examiner's indication that claims 2 and 4-6 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

In this Amendment, claim 1 has been amended to clarify that "said subdecoder region [is] located between said intersection regions." Adequate descriptive support for the amendment can be found in, for example, Fig. 2 and relevant description of the specification. In addition, claim 1 has been amended for better form by replacing the recitation "said sense amplifier" with --a sense amplifier formed by said sense amplifier-forming element--. Care has been exercised to avoid the introduction of new matter.

**Claims 1 and 3 have been rejected under 35 U.S.C. §102(b) as being anticipated by Kitsukawa et al.**

In the statement of the rejection, the Examiner asserted that Kitsukawa et al. discloses a system with meshed power and signal buses on a cell array identically corresponding to what is claimed.

It is established that the factual determination of lack of novelty under 35 U.S.C. §102 requires the identical disclosure in a single reference of each element of the claimed invention, such that the identically claimed invention is placed into the possession of one having ordinary skill in the art. *Helifix Ltd. v. Blok-Lok, Ltd.*, 208 F. 3d 1339, 54 USPQ2d 1299 (Fed. Cir. 2000); *Electro Medical Systems S.A. v. Cooper Life Sciences, Inc.*, 34 F.3d 1048, 32 USPQ2d 1017 (Fed. Cir. 1994).

Based on the above legal tenet, Applicant submits that Kitsukawa et al. does not disclose a semiconductor memory device including all the limitations recited in claim 1, as amended, within the meaning of 35 U.S.C. §102. Specifically, the reference does not disclose a semiconductor memory device containing “a plurality of sense amplifier driver elements each arranged in said subdecoder region located between said intersection regions,” recited in claim 1 (emphasis added).

Fig. 2 of Kitsukawa et al. appears to disclose that subarrays 18a, 18b including memory cells are arranged in matrix, spaced apart from each other in a row direction and in a column direction. It also appears that in Fig. 2, areas where address subdecoder 20a, 20b are disposed correspond to a claimed “plurality of subdecoder regions,” areas where sense amplifiers are disposed correspond to a claimed “plurality of sense amplifier regions,” and intersection areas 24a-24f correspond to a claimed “plurality of intersection regions.” However, the reference does not disclose that a sense amplifier driver 100a considered to correspond to the claimed plurality of sense amplifier driver elements is disposed in the area where subdecoder 20a, 20b are disposed, whereas each of the claimed plurality of sense amplifier driver elements is arranged in the subdecoder region located between the intersection regions. In fact, Kitsukawa et al. clearly indicates, “Both of the sense amplifier circuits 98a-98b are connected to a sense amplifier driver 100a, which is located in the intersection area 24a” (column 8, lines 48-50) (emphasis added).

In such an arrangement disclosed in Kitsukawa et al., for example, a reduced number of divisions in the direction of a word line is accompanied by a reduced area of an intersection region, and if a sense amplifier driver is arranged only at the intersection region, the area for arranging the sense amplifier driver may insufficiently be ensured. If the intersection region were increased to have an area to allow the sense amplifier driver to be arranged only at the region, the semiconductor

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device would have an increased chip area. The semiconductor memory device cannot have a reduced chip area (see page 9, line 29 to page 10, line 9 of the specification).

Accordingly, Applicant submits that Kitsukawa et al. does not disclose a semiconductor memory device containing all the limitations recited in claim 1, and therefore, does not have identical disclosure of each element of the claimed invention in the meaning of 35 U.S.C. §102.

It is also noted that a dependent claim is not anticipated if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claim. Therefore, claim 3 is patentable because it includes all the limitations of independent claim 1. The Examiner's additional comments with respect to claim 3 do not cure the argued fundamental deficiencies of Kitsukawa et al.

Therefore, Applicant respectfully solicits withdrawal of the rejection of claims 1 and 3 under 35 U.S.C. §102(b) and favorable consideration thereof.

**Conclusion.**

Accordingly, it is urged that the application is in condition for allowance, an indication of which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including

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extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT WILL & EMERY LLP

A handwritten signature in black ink, appearing to read "Tomoki Tanida", written over the printed name.

Tomoki Tanida

Recognition under 37 C.F.R. 10.9(b)

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